Quantum circuit optimizations by qubit mapping

Zihao Sun

**Introduction**

In pursuit of optimizing the mapping of logical quantum circuits onto physical circuits in Noisy Intermediate-Scale Quantum (NISQ) devices, this research aims to resolve the question of : How can the transformation of logical quantum circuits to physical circuits in NISQ devices be optimized, particularly in minimizing the insertion of auxiliary two-qubit gates (SWAP gates)? It focuses on introducing a novel algorithm anchored in subgraph isomorphism and filtered depth-limited search. The objectives are manifold: establishing initial mappings through subgraph isomorphism, maximizing executable two-qubit gates per SWAP operation through a filtered depth-limited search, and empirically evaluating the proposed algorithm against existing methods.

**Background**

In the introductory background of the research, a comprehensive review focusing on the fundamental concepts of quantum gates and quantum circuits is systematically presented. This is meticulously followed by a detailed exploration and clarification of the intricate dependency graphs associated with logical circuits. Furthermore, the study illuminates the methodological process involved in segregating the logical circuit into discrete, well-defined layers, leveraging the insights drawn from the analysis of the previously discussed dependency graphs. This sequential presentation and in-depth discussion are instrumental in fostering a robust understanding of the hierarchical structuring and functional dependencies inherent within logical circuits.

**2.1 Quantum Gates and Quantum Circuits**

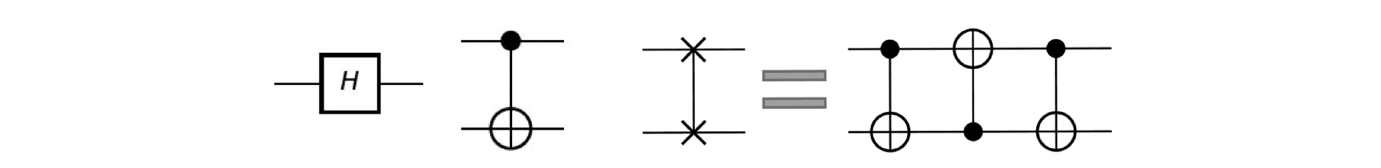
This section is dedicated to a detailed discussion of the core principles underlying quantum gates and quantum circuits, which hold pivotal roles in the manipulation and computation of quantum information. At the heart of quantum computing lies the qubit, a quantum analogue of the classical bit. Unlike the classical bit, which is confined to a state of either 0 or 1, a qubit flourishes in a superposition of states, represented as |ψ⟩ = α|0⟩ + β|1⟩, where the complex probability amplitudes α and β adhere to the condition |α|^2 + |β|^2 = 1. Superposition states thus magnifies the computational potency of quantum computing through strategic exploitation of quantum superposition.

Quantum computations pivot on the operation of quantum gates on qubits. A hierarchy of gates exists, ranging from intricate multi-qubit gates, which are decomposable into simpler fundamental gates, to basic one or two-qubit gates. A notable accomplishment in the field is the approximation of any quantum gate with remarkable precision using a specific assortment of single-qubit gates coupled with Controlled NOT CNOT gates (Linke et al., 2017).

Figure 1 illustrates three quintessential gates: Hadamard gate H, CNOT gate, and SWAP gate. The Hadamard gate, a unitary transformation, acts on individual qubits, ushering them into a state of balanced superposition. It meticulously maps |0⟩ to |+⟩ and |1⟩ to |-⟩. CNOT and SWAP gates are instrumental two-qubit gates. The CNOT gate executes a conditional bit-flip, contingent on the control qubit being in state |1⟩. Conversely, the SWAP gate interchanges the states of paired qubits, delineated mathematically as transforming states |a⟩|b⟩ to |b⟩|a⟩, where a and b belong to the binary set {0, 1}.

For NISQ devices, the native incorporation of SWAP gates is commonly absent, necessitating the conjunctive use of three CNOT gates for their realization.

The architectural blueprint of quantum algorithms is predominantly actualized through quantum circuits, comprising elemental components such as input qubits, quantum gates, and classical registers (Šupi et al., 2018). This paper characterizes a quantum circuit as an ordered pair (Q, C) , where Q signifies the ensemble of qubits employed, and C denotes the orchestrated sequence of quantum gates, underscoring the quintessence of input qubits and quantum gates in the qubit mapping discourse.

  
  
*Fig. 1. Hadamard, CNOT, and SWAP gate (from left to right).*

**2.2 Detailed Overview of Dependency Graphs and Layer Formation**

Within the realm of logical circuits, denoted as LC = (Q; C), there exists a nuanced hierarchy amongst two-qubit gates, stipulating that these gates are not universally independent entities. Instead, they exhibit interdependencies that play a pivotal role in their operational sequence. A two-qubit gate, referenced as g1, is described as being dependent on a second gate, g2, under conditions where the execution of g2 is a prerequisite for the operation of g1.

This hierarchical dependency manifests in scenarios where g2 is sequentially positioned ahead of g1 in the context of C, coupled with their sharing of a common qubit. Moreover, such dependencies can be propagated transitively; for instance, g1 could be dependent on a third gate, g3, which is, in turn, dependent on g2.

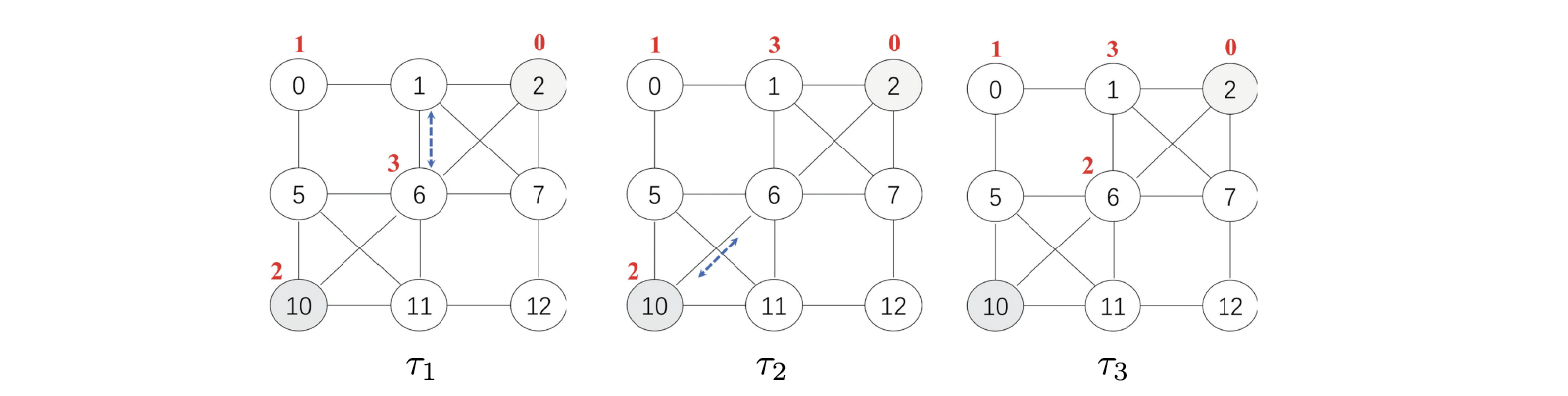
Delving into the intricacies of direct dependencies, a gate g1 is explicitly defined as having a direct dependency on gate g2 when no intervening gates that also share the identical common qubit are present between them within the sequential construct of C (Wagner et al., 2023).

A strategic approach employed for the visualization and delineation of these hierarchical gate dependencies within a logical circuit is through the formulation of a directed acyclic graph, known as the dependency graph. Within this graph, individual nodes are representative of two-qubit gates. Direct dependencies between these gates are articulated through directed edges, establishing a clear depiction of operational precedence and inter-gate relationships.

Initiating the structural layers within the logical circuit, the foremost layer, symbolized as F(LC) or L0(LC), is comprised of two-qubit gates devoid of any antecedent gates within the dependency graph, signifying their autonomous operational capacity (Li et al., 2020).

Following the establishment of the initial layer, subsequent layers such as L1(LC) evolve through a systematic process of gate eliminations from the preceding layer within the logical circuit LC. This iterative methodology perpetuates throughout the logical circuit, facilitating the demarcation of layers Lk(LC) where k is incrementally extended, reflecting the progressive refinement and structuring of the logical circuit’s dependency hierarchy.  
This can be shown in the Fig 2 graph where gate g2 can be executed only after g0

and g1.



*Fig. 2. Qubit mappings are represented as Ti : {q0, q1, q2, q3} -> V for i = 1, 2, 3. In this representation, T2 is derived from T1 by applying SWAP(1,6), and T3 is subsequently obtained from T2 by employing SWAP(6,10). Here, SWAP(1,6) is a simplified notation used instead of SWAP(v1, v6).*

**Research significance and innovation**

This research will hold significant relevance in the quantum computing domain, promising enhanced efficiency and reliability of quantum circuits within NISQ devices, thereby benefiting stakeholders like quantum computing theorists, engineers, and diverse industries exploring quantum solutions. However, complexities, such as advanced knowledge prerequisites and computational demands, may pose challenges in implementing the new algorithm. Fundamentally, this research aspires to revolutionize quantum circuit mapping approaches, yielding a more efficient and operable mapping process as evidenced by empirical results, which highlight a marked reduction in necessary auxiliary two-qubit gates and a leap in algorithmic efficiency and performance compared to existing methodologies.

**Research method**

The research adopts a post-positivism paradigm, utilizing a quantitative methodology focused on the empirical evaluation of a newly proposed algorithm in the context of quantum computing. The proposed algorithm’s effectiveness and efficiency are meticulously analyzed through a comparative performance analysis method, wherein its operational efficacy in transforming logical quantum circuits to physical circuits in Noisy Intermediate-Scale Quantum (NISQ) devices is rigorously tested and validated against established algorithms. Data is predominantly collected through extensive algorithmic testing and experimentation across various quantum circuits and configurations, ensuring a comprehensive evaluation process. Despite being algorithm-centric research without human participants, potential barriers to effective data collection may encompass technological constraints and the rapid evolution of quantum computing algorithms and technologies. The entire research methodology, from algorithm evaluation to data collection and analysis, is meticulously aligned with the study’s objectives, ensuring a coherent, objective-driven research approach. The conclusions drawn from the research underscore the algorithm’s adaptability, effectiveness, and areas for future refinement and enhancement, corroborating the empirical robustness of the study’s methodological framework.

**Reference**

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